UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
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ART UNIT	PAPER NUMBER
2181	

NOTIFICATION DATE	DELIVERY MODE
07/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOmail3@bakerbotts.com
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	Application No.	Applicant(s)
Office Action Summary	10/824,874	BALLEW ET AL.
	Examiner	Art Unit	
	Vincent Lai	2181	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>29 May 2007</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-27</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-27</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>See Continuation Sheet</u>.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____ .

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :11/13/06, 3/2/07, 3/26/07, & 5/18/07.

DETAILED ACTION

Information Disclosure Statement

1.   The information disclosure statements (IDS) submitted on 8 March 2006, 13

November 2006, 29 December 2006, 2 March 2007, 26 March 2007, and 18 May 2007

have been considered by the examiner.

Response to Amendment

2.   35 USC 112 rejections are withdrawn after considering amendments.

Response to Arguments

3.   Applicant has correctly pointed that item M of the IDS received 13 November

2006 has been received by the office and thus the IDS has been considered.

4.   Applicant's arguments filed 29 May 2007 have been fully considered but they are

not persuasive.

Applicant on pages 7 and 8 argue that although Karpoff teaches "a switch

comprising eight or more ports and at least two processors...Karpoff would still fail to

disclose, teach, or suggest that one device is a motherboard and that both the switch

and the controller device were integrated on the one motherboard.

It is noted that Applicant appears to consider figure 4a to be the only embodiment taught by Karpoff. It is noted that the cited sections of the rejections encompass the various embodiments taught by Karpoff and consideration of such embodiments do show the limitations of the claims. It is noted that figures 12a and 12b appear to resolve the apparent deficiencies argued by the Applicant.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.   Claims 1-7, 9-14, and 21-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Karpoff (U.S. Patent Application # US 2001/0049740 A1).

As per **claim 1**, Karpoff discloses a node comprising:

a motherboard (See figure 4A: Server 20 is contained on a board);

a switch comprising eight or more ports (See figure 4A: IB Switch 26), the switch integrated on the motherboard (See paragraph 104: A switch and a controller device are contained on one device); and

at least two processors, each processor communicably coupled to the integrated switch and integrated on the motherboard (See figure 4A and paragraph 22 and 43: The can be many processors 30 that are able to interact and communicate).

As per **claim 2**, Karpoff discloses the node of claim 1, each processor coupled to the integrated switch through a Host Channel Adapter (HCA) (See figure 4A: HCA 22).

As per **claim 3**, Karpoff discloses the node of claim 2, each processor further coupled to the integrated switch through a peripheral component interconnect (PCI) bridge (See paragraph 111: PCI is an acceptable type of messaging protocol).

As per **claim 4**, Karpoff discloses the node of claim 1, at least two of the processors communicably coupled directly to each other via a link supporting processor-to-processor communication (See paragraph 22 and 43: Devices can communicate and share data directly without the server system).

As per **claim 5**, Karpoff discloses each processor communicably coupled to the integrated switch through a Northbridge (See figure 4A: A Northbridge is memory controller 28).

As per **claim 6**, Karpoff discloses the node of claim 1, the integrated switch operable to communicate input/output (I/O) messages at a bandwidth substantially similar to power of the processors (See paragraph 116: The streaming manager is capable of fulfilling bandwidth requests).

As per **claim 8**, Karpoff discloses the node of claim 1, the integrated switch operable to:

communicate a first message from a first of the two or more processors (See paragraph 22 and 43: Devices can communicate with any other device and share data directly without the server system); and

communicate a second message from a second of the two or more processors, the first and second message communicated in parallel (See paragraph 22 and 43: Devices can communicate and share data directly without the server system and more than one set of devices can communicate at the same time).

Claims 9-14 are rejected for reasons similar to claims 1-6. Claims 9-14 are related to a system comprising a plurality of interconnected nodes, the nodes being claimed in claims 1-6. An interconnection of nodes can be seen in figure 4B of Karpoff.

Claims 21-26 are rejected for reasons similar to claims 1-6. Claims 9-14 are related to a method of using the nodes being claimed in claims 1-6.

Claim Rejections - 35 USC § 103

6.   Claims 7,15-20, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karpoff in view of Pechanek et al (U.S. Patent # 6,167,502), herein referred to as Pechanek.

As per **claim 7**, Karpoff teaches the node of Claim 1,the integrated switch comprising twenty-four ports (See paragraph 103: Karpoff teaches that a plurality of devices are attached to the switch and does not limit the amount of deceives attached to it, thus leaving twenty-four or another other number of ports are possible.)

Karpoff does not teach a toroidal topology.

Pechanek teaches and enabling a toroidal topology comprising four dimensions (See column 15, lines 31-40: A 4D topology is taught by Pechanek).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Karpoff with Pechanek because both are related to array processing, but where as Karpoff is array processing done in a network setting, Pechanek is array processing done in an enclosed environment. Both try to take advantage of multiple processors working together to increase computing power via data switches. Since Karpoff is done in a network setting, a 4D toroidal setting is not explicitly taught since such a network setting is capable of being much more complicated. Pechanek can teach a 4D toroidal setting since it is somewhat confined structurally. One having ordinary skill in the art would appreciate the simpler method of a 4D toroidal topology and thus would be inclined to limit Karpoff in a way similar to that in Pechanek in order to reduce complexity.

Claim 15 is rejected for reasons similar to claim 7. Claim 15 is related to a system comprising a plurality of interconnected nodes, the nodes being claimed in claims 7. An interconnection of nodes can be seen in figure 4B of Karpoff.

As per **claim 16**, Karpoff teaches the system of claim 9.

Karpoff does not teach the plurality of nodes arranged in a topology.

Pechanek does teach the plurality of nodes arranged in a topology, the topology enabled by the integrated fabric of each node (See abstract).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Karpoff with Pechanek because both are related to array processing, but where as Karpoff is array processing done in a network setting, Pechanek is array processing done in an enclosed environment. Karpoff is silent on topology, but given the manner in which each node is fashioned, there must exist a topology of some sort. Pechanek explicitly teaches a topology and thus one having ordinary skill in the art would recognize some semblance of a topology taught by Karpoff and be able to apply topology using Pechanek.

As per **claim 17**, Karpoff and Pechanek teach the system of claim 16.

Karpoff does not teach the plurality of nodes arranged in a topology.

Pechanek does teach the plurality of nodes arranged in a topology, the topology comprising a hypercube (See column 15, lines 31-40: Pechanek teaches a 4D hypercube).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Karpoff with Pechanek because both are related to array processing, but where as Karpoff is array processing done in a network

setting, Pechanek is array processing done in an enclosed environment. Karpoff is silent on topology, but given the manner in which each node is fashioned, there must exist a topology of some sort. Pechanek explicitly teaches a topology and thus one having ordinary skill in the art would recognize some semblance of a topology taught by Karpoff and be able to apply topology using Pechanek.

As per **claim 18**, Karpoff and Pechanek teach the system of claim 16.

Karpoff does not teach the plurality of nodes arranged in a topology.

Pechanek does teach the plurality of nodes arranged in a topology, the topology comprising a folded topology (See column 15, lines 31-40: Pechanek teaches a folded array).

, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Karpoff with Pechanek because both are related to array processing, but where as Karpoff is array processing done in a network setting, Pechanek is array processing done in an enclosed environment. Karpoff is silent on topology, but given the manner in which each node is fashioned, there must exist a topology of some sort. Pechanek explicitly teaches a topology and thus one having ordinary skill in the art would recognize some semblance of a topology taught by Karpoff and be able to apply topology using Pechanek. Although Pechanek refers to a folded topology as prior art, one having ordinary skill in the art would still be able to take the teachings of the prior art and combine it with Karpoff to achieve a folded topology.

As per **claim 19**, Karpoff teaches the system of claim 9.

Karpoff does not teach the plurality of nodes arranged in a topology.

Pechanek system of claim 9, a first node of the plurality of nodes interconnected to a second node of the plurality of nodes along an X axis, a third node of the plurality of nodes along a Y axis that is perpendicular to the X axis, a fourth node of the plurality of nodes along a Z axis that is perpendicular to the X and Y axes, and a fifth node along a diagonal axis that is oblique to one or more of the X, Y, and Z axes (See column 15, lines 31-40: Pechanek teaches a 4D hypercube and thus would have this topology).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Karpoff with Pechanek because both are related to array processing, but where as Karpoff is array processing done in a network setting, Pechanek is array processing done in an enclosed environment. Karpoff is silent on topology, but given the manner in which each node is fashioned, there must exist a topology of some sort. Pechanek explicitly teaches a topology and thus one having ordinary skill in the art would recognize some semblance of a topology taught by Karpoff and be able to apply topology using Pechanek.

As per **claim 20**, Karpoff and Pechanek teach the system of claim 19.

Karpoff does not teach the plurality of nodes arranged in a topology.

Pechanek does teach the connection between the first node and the fifth node operable to reduce message jumps among the plurality of nodes (See column 15, lines 31-40: All elements in the hypercube are connected).

It would have been obvious to a person having ordinary skill in the art at the time

the invention was made to have modified Karpoff with Pechanek because both are

related to array processing, but where as Karpoff is array processing done in a network

setting, Pechanek is array processing done in an enclosed environment. Karpoff is

silent on topology, but given the manner in which each node is fashioned, there must

exist a topology of some sort. Pechanek explicitly teaches a topology and thus one

having ordinary skill in the art would recognize some semblance of a topology taught by

Karpoff and be able to apply topology using Pechanek.

Claim 27 is rejected for reasons similar to claims 7. Claim 27 is related to a

method of using the nodes being claimed in claims 7.

Conclusion

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

vl
July 12, 2007

Vincent Lai
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER